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Wafer Level Packaging Technology for Optical Imaging Sensors

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Abstract

Moore's Law postulated that the number of transistors per chip would double roughly every 2 years. In parallel with the increased device density within a chip, there is an increased overall functionality. This trend can be seen in applications such as MEMS, RF circuits, where sensors, microactuators are integrated with digital and analog electronic components. This complexity leads to smaller bond pads on devices and packaging challenges. One of the requirements for the packages of image sensors and MEMS devices (such as RF- and AeroMEMS) or solar cells is the backside contact. The optical devices require an interface with environment without any restriction caused by the packages and on the other hand require a protection against the environment. Figure 1 shows main differences between IC package and package of an imaging sensor. In this paper, we discuss the two existing wafer-level-packaging technologies used already in mass production and give process details about our new WLP technology using via contacts between front end pads and redistribution.

Keywords: image sensors, wafer level chip-scale packaging, TSV, TWV, back side contact, MEMS

1. Motivation and achievement

The digital camera market is one of the still-expanding markets and driving force for wafer-level-packaging technologies. Packaging has been known to add as much as 30% of imaging sensors.

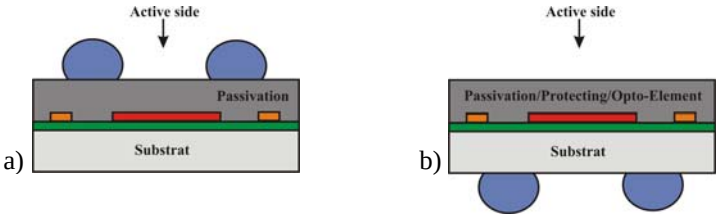

Fig. 1. Differencies between traditional IC package a), and image sensor package b).

TSV (Through Silicon Vias) [1] approach provides the shortest and most plentiful z-axis connections. TSV technology offers some potential benefits such as reducing connection lengths between blocks, enabling high-density and high-aspect-ratio connections. This technology is still at R&D stage but is in focus as a potential

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solution for WLP technology with high priority. There are two existing WLP technologies used in high volume production: a) using T-contacts WLP [2] and b) using L-contacts WLP [3]. In this work we developed new packaging technology using via contacts. We already presented the technology schematically in one earlier paper [4]. The aim of via-contacts WLP [4] is to avoid all disadvantages of both above-mentioned technologies.

2. T-contact and L-contact WLPs

This two technologies are described in details in [2][3]. Both technologies need the so called extension pads to make electrical contact from redistribution on back side of the chip and front-end circuits. So all contacts and leads are located at chip boarders (figure2 and 3), what makes this area very sensible against mechanical loads, temperature and humidity. The contacts are realized in dicing streets between the chips on wafer. This streets are ctreated by using dicing or plasma etching in high rate plasma chambers. The uniformity and quality of dicing and etching of such long features in silicon is bad, which normally leads to lower yield. Chipping and etch products such as CF-polymers typical for this processes can also reduce the quality and reliability of the packages.

2.1. T-contact WLP

A short process flow of this technology is given in figure 2. The silicon wafer is first bonded onto glass wafer by using epoxy. After that the silicon is thinned to allow maximum performance of image sensors. In the next step the scribe line is created by using etching in a high rate plasma chamber. Second glass wafer is then bonded on the grinded and smoothed side of the silicon wafer. After deposition and structuring of barrier layers, notch is performed by dicing. In this step the extension pads are also cut and ready to be contacted. Metallization is done by using sputtering of AlSiCu. Redistribution and bumping could be done by using standard processes. In this technology the lead and the extension pad form a T (figure 2).

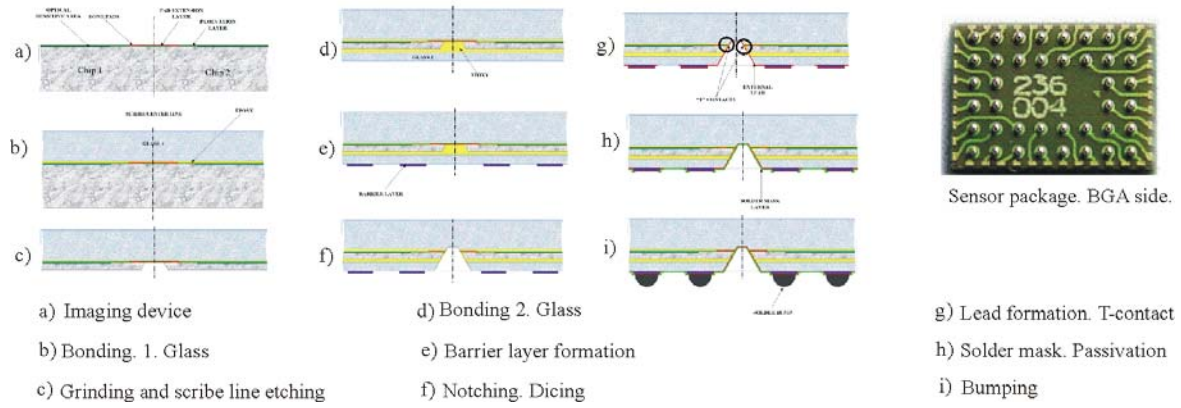

Fig. 2. Process flow of the T-contact WLP [2] and sensor package.

The thickness of the front-end metallization defines the physical contact area between them, which can varied between some hundred nanometers up to 2µm. Chipping and roughness are typically in this range or even worse and can cause breakage between lead and pads. The cost per die is increased since two glass wafers are needed. The total thickness of the sandwich (Glass/Si/Glass) is high in compare to other technologies. Other disadvantage of this technology is the long dicing time after second bonding process.

2.2. L-contact WLP

The process flow of this technology is given in figure 3. The purpose of this technology is to avoid the small T-contact in the above described technology, which is indicated as main failure source in the T-contact WLP. In this case extension pad and lead form a L (figure 3). But like the T-Contact WLP the contacts are located in dicing

street, so they can be damaged during processing. Moisture can penetrate in the passivation layers in this area, which can lead to delamination or corrosion of the layers. The silicon wafer is first bonded onto glass wafer. After thinning the silicon wafer, contact windows between chips are formed by using plasma etching. A thin PECVD silicon oxide was deposited to passivate the silicon surface. In the next step the front end passivation was opened by using plasma etching or wet etch by using BHF. Metallization was done by using sputtering of AlSiCu. Redistribution and bumping could be done by using standard processes.

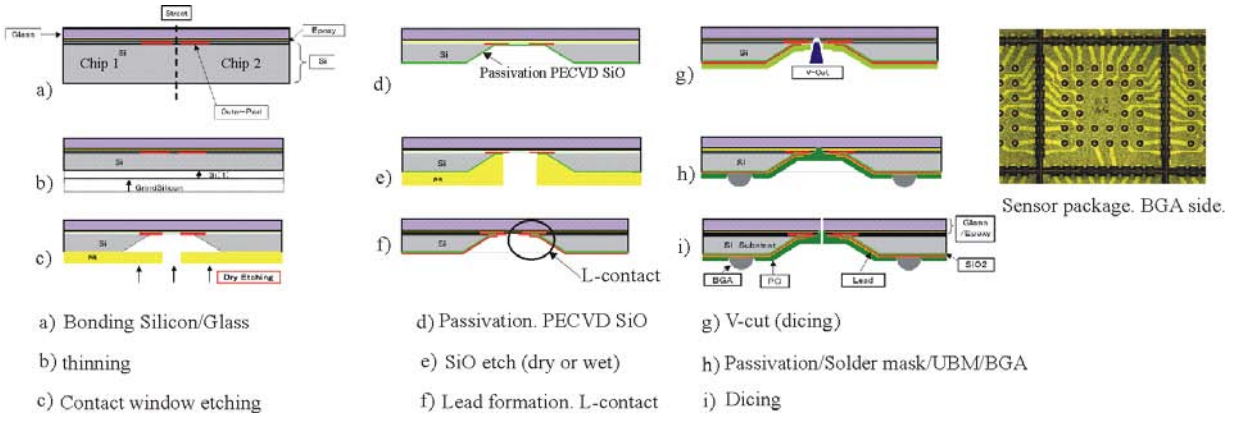

Fig. 3. Process flow of the L-contact WLP [3] and sensor package.

3. The new via-contact WLP

Process flow of Via-contact WLP is shown in figure 4. In this technology the extension pads are not needed, so no additional design rules are nessesary. Via contacts can be placed directly on front-end pads and fulfill all requirements. The contact areas are not placed in dicing streets so they don't face the mechanical stresses during the dicing or notching steps. Similar to T- and L-contact WLPs, the silicon wafer is first bonded onto glass wafer by using epoxy. After mechanical grinding the silicon wafer to reduce the silicon thickness down to ca. 120µm, a wet etch (spin etch by using $HF/HNO_3/H_2SO_4/H_3PO_4$ mixture) is performed to remove the top silicon layer (~30-35µm) with high crystal damages. This silicon layer is normally under very high mechanical stress, which can bend the silicon-glass sandwich and influence the sensor performances, or can cause delamination of passivation layer deposited on top. After that, the vias for the contact and trenches between dies are formed by using plasma etching [5] in one step. New plama tools allow high etching rate, high throughput and good uniformity. Using electrostatically working wafer chucks instead of mechanical clamping reduces the exclusion area on wafers and avoid any mechanical damages and contamination on wafer surface.

The shape and quality of the vias have very big influences on package reliability. In this work new etch techniques were developed to create features with tapered side walls in silicon without any overhang. Vias and trenches with tapered side walls are needed to make lithography and deposition processes inside this features possible. Vias and trenches are shown in figure 5. Optimal side wall angle is about 70° for 80µm deep vias. In order to remove any etch products from DRIE (such as SiF components or C_xF_y polymers) or roughness inside the vias (which can cause delamination of passivation layer inside vias) a short wet etch step ($HF/HNO_3/H_2SO_4/H_3PO_4$ system too but with different ratios from mixture used in the first wet etch) has been done to remove about 5µm of silicon. It improves the adhesion and reliability of the passivation layer deposited in the next step. Other purpose of this step is to round the top sharp corner of vias and trenches to have better coverage of lead and IDL layers at this area. In the next step a PECVD SiO (100% Silan, 120°C) layer of 2µm was deposited. After that an IDL (normally polymer like JSR or BCB is used) was coated by using spray coating to prevent any electrical shorts between leads and silicon and to serve as a compensation layer for any mechanical or thermal stresses. In order to make contact between the front-end pads and leads, the PECVD SiO layer, the front-end customer passivation and the IDL were opened at the bottom of the vias by using plasma etching. No charging effects are observed during this step. Except the lithography for silicon etching, all lithography steps are done by using the new spray coating technique. In the

next step, AlSiCu or AlCu is deposited for lead formation by using standard sputtering. A second polymer (BCB) is applied to serve as passivation for the metal leads and as solder mask. The BGA on the back side can be adapted to the specific requirements of board level assembly. For solder balls Ni-Au UBM and lead-free SnAgCu are used.

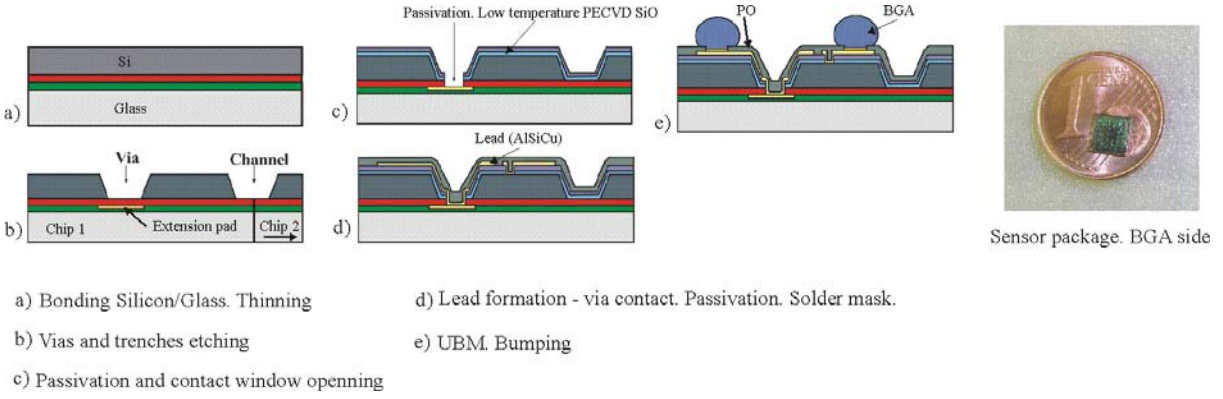

Fig. 4. Process flow of the Schott via-contact WLP [4] and package of a 3.2 Meg Pixel sensor.

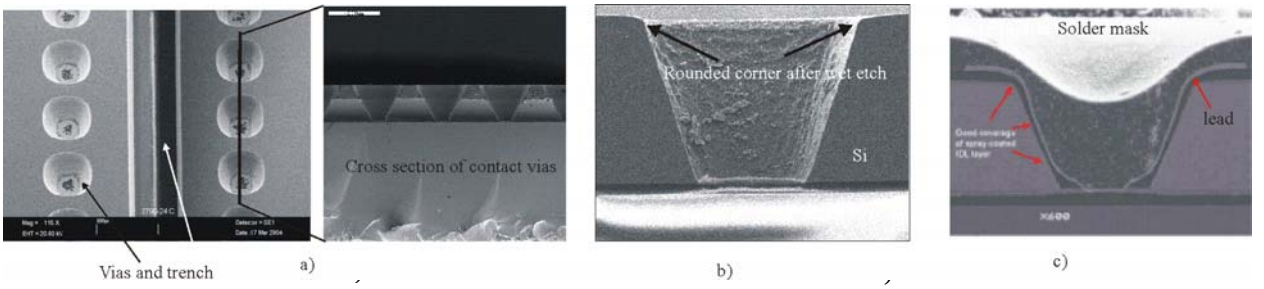

Fig. 5. Vias and dicing street after plasma etching a), and via after plasma etching + short wet etch showing rounded top corner b). Cross section view of a via after complete process c).

In this process, a typical yield of 98% is achieved on 8-inch wafers. Extensive reliability tests according to JEDEC standards (THS – 85°C at 85% RH and TCT - -40°C/+85°C) have been curried out. It can be shown that the reliability test chips can survive up to THS 1000 hours. As for TCT, there were no abnormalities found.

4. Conclusion

Three technologies used for packaging of image sensors are discussed in this paper. Disadvantages with T- and L-contact WLPs can be avoided by using via contact WLP. Via contact WLP shows very good yield, high throughput and reliability performances.

References

1. J. Knickerbrocker et al, “Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch interconnection”, IBM J. Res. Dev. 49 (4/5), 2005, pp. 725-754.

2. A., Badihi et al., “Ultrathin wafer level chip size package”, IEEE Trans. On Advanced Packaging, vol. 23, No. 2, May 2000, pp. 212-214.

3. T. Noma et al., “Semiconductor device and manufacturing method there of”, *US Patent 2003/0230805 A1, 2003*.

4. J. Leib et al., “New wafer-level-packaging technology using silicon-via-contacts for optical and other sensor applications”, *Digest Tech. Papers ECTC 2004 Conference*. Las Vegas, USA, 2004.

5. H.-D. Ngo et al, “Plasma etching of tapered features in silicon for MEMS and Wafer Level Packaging Applications”, Conference Proceeding iMEMS, Singapore 2006, pp. 271-276.